ECEn 452 – Semiconductor Devices Lab

Week 10: "Source and Drain Vias"

Objectives

Introduction

In Week 9 you etched features into your oxide in order to define your gate region and grew your gate oxide. This week you are going to have to align your source and drain via features on a new lithography mask with the pre-existing features on your wafer. You will etch through the oxide below these via features and then deposit Aluminum over the surface of the wafer. This metal will contact your source and drain region through the vias you created. This aluminum will also serve as the contact to the gate region of your MOSFET.

By the end of this lab, your four processing wafers should have source and drain vias and aluminum coating their entire surfaces. This lab requires repeating many of the processing steps you are already familiar with. To maximize your wafer throughput, different group members could handle different objectives, although everyone should get a chance to practice with the aligner.

Prelab questions

1. According to the background reading, what characterizes a good contact for electronic applications?

2. How long will it take to deposit 300nm of Aluminum on a wafer if you want to ensure no oxidation?

3. What will be the effect of under etching the drain and source vias?

4. What would the I-V curves look like if the vias were under etched?

5. How will you know when your vias have been sufficiently etched?

Major Objectives

1. Photoresist Application:

Using your standard lithography process, apply photoresist to your 4 process wafers. (Be sure to dehydration bake!)

2. Mask Alignment:

Mask alignment will be done using the Alignment tool that you have previously used to expose patterns in your wafers and the "Source and Drain Vias" Mask. Have the lab supervisor show you how to manipulate the position of the wafer under the mask and how to position the "alignment marks" so that they line up. You will find that the

most difficult part of alignment is getting the rotation angle of your wafer just right. Alignment takes patience especially when you do it for the first time so try not to get frustrated. Let everyone in your group do some alignment. Align and expose all 4 process wafers, and then develop the pattern.

3. Alignment Tolerance:

Using an optical microscope, estimate the alignment tolerance for your wafers. Map your alignment tolerance over the entire wafer surface and document it. You might notice that some areas look pretty well aligned while others do not – this is a sign that you did not get that rotation angle exactly right. If the alignment tolerance is too poor, strip off the photoresist and repeat the lithography steps. Consult the lab supervisor as to what would be “too poor.”

4. Plasma Etching – Descum:

When you are satisfied with the alignment of your wafer, descum it for about 15 seconds in the oxygen plasma in preparation for oxide etching.

5. Oxide Etching:

Silicon dioxide etching is done using BOE (Buffered oxide etch or Buffered HF). Because HF is dangerous, you need to be very careful during this processing step. BOE etches thermally grown silicon dioxide at 100 nm per minute quite accurately, but does not etch silicon.

6. Plasma Etching – Bulk PR Removal:

Use the parallel plate etcher and an oxygen plasma to remove the photoresist coating your four silicon wafers after completing Objective 5. You will need to etch these wafers for a longer time to remove the thick photoresist (12 minutes at 250 Watts). Be sure to check under a microscope to ensure the photoresist is gone.

7. Metal Deposition:

In this objective you will evaporate 300 nm of Aluminum onto the wafer surface. Before loading your wafers into the evaporator, give them a quick dip in BHF to remove any residual oxide. Also dip them in a solution of $HCl:H_2O$ (2:1) for a few seconds to remove any organic residue. Deposit metal in the same way you did in Week 2. This metal will serve as your contacts to the gate, source, and drain for the MOSFET.

8. Inspect the deposited Aluminum under a microscope:

Is there any visual difference between the aluminum sitting on top of the silicon dioxide compared to the aluminum contacting the silicon directly?