ECEn 452 – Semiconductor Devices Lab

Week 11: "Metal Contacts"

Objectives

Introduction

In Week 10 you etched vias into your oxide to allow for metal connections to your source and drain regions, then deposited aluminum over the entire structure. This week you are going to define your metal contacts to the source, drain, and gate regions. To do this you must align your contact features on a new lithography mask with the pre-existing features on your wafer. When you have done the proper lithography and etched your metal, you will then anneal the contacts – this will be similar to what you did in Week 5. By the end of this lab, your four processing wafers should have annealed metal contacts and be ready for electrical testing. Due to the serial nature of this lab, different group members could handle different objectives to maximize your throughput, although everyone should get a chance to work with the aligner.

Prelab Questions

1. What are the possible effects of residual oxide over the source, gate, and drain regions of the MOSFET when the metal contacts are defined?
2. What can happen if enough metal is not applied in making the contacts?
3. What would be the result if the contact for the gate overlapped the source or drain?
4. What would happen if the metal were etched for the wrong amount of time?

Major Objectives

1. Photoresist Application:

Using your standard lithography process, apply
photoresist to your 4 process wafers (be sure to dehydration bake!).

2. Mask Alignment:

Mask alignment will be done using the Alignment tool that you have previously used to expose patterns on your wafers and the "Contacts" Mask. Have the lab supervisor show you how to manipulate the position of the wafer under the mask and how to position the "alignment marks" so that they line up. You will find that the most difficult part of alignment is getting the rotation angle of your mask just right. Alignment takes patience especially when you do it for the first time so try not to get frustrated. Let everyone in your group do some alignment. Align and expose all 4 process wafers, and then develop the pattern.

3. Alignment Tolerance:

Using an optical microscope, estimate the alignment tolerance for your wafers. Map your alignment tolerance over the entire wafer surface and document it. You might notice that some areas look pretty well aligned while others do not – this is a sign that you did not get that rotation angle exactly right. If the alignment tolerance is too poor, strip off the photoresist and repeat the lithography steps. Consult the lab supervisor as to what would be "too poor."

4. Plasma Etching – Descum:

When you are satisfied with the alignment of your wafer, descum it for about 15 seconds in the oxygen plasma in preparation for metal etching.

5. Aluminum Etching:

Aluminum etching is done using the Aluminum etchant used earlier in Lab 5. Use the etching recipes you developed in that lab to etch through your layer of aluminum. This should involve heating the etchant to get a reasonable etch rate. Make sure you inspect your wafers when the etch is complete to ensure that you have removed all the necessary aluminum.

6. Plasma Etching:

Bulk PR Removal. Use the Solitec Spinner to remove the photoresist coating from your four silicon wafers after completing Objective 5. Be sure to check under a microscope to ensure the photoresist is gone.

7. Metal Annealing:

When your wafers have been cleared of photoresist, anneal them in the tube furnace. Choose the annealing conditions that were optimal from Lab 5. Your main goal is to get an ohmic contact on your source and drain, so you want the contact resistance to be as low as possible.

8. Inspect your aluminum contacts under a microscope:

Is there anything different after annealing compared to before annealing? Does the aluminum on top of the oxide look any different than the aluminum directly contacting the silicon?

Conclusion

Your MOSFETs should now be complete! They are now ready for electrical testing to see how your processing really went.