ECEn 452 – Semiconductor Devices Lab
Week 12/13
"MOSFET Characterization"

BACKGROUND READING

A Complete MOSFET

Congratulations! You have completed a MOSFET from scratch. The steps taken in making your transistor may seem repetitive, but precision and care in doing them is essential. For a recap of all the steps taken in fabricating your MOSFET, see the following website:

http://jas.eng.buffalo.edu/education/fab/NMOS/nmos.html

Especially take note of the final product, top view, since this is what you will be looking for under a microscope. We will now go through some information you will need to be familiar with before completing this lab.

Transconductance

Transconductance is an expression of the performance of field-effect transistor (FET). In general, the larger the transconductance figure for a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant.

Formally, for an FET, transconductance is the ratio of the change in drain current to the change in gate voltage over a defined, arbitrarily small interval on the drain-current-versus-gate-voltage curve.

The symbol for transconductance is g_m. The unit is the siemens (S), the same unit that is used for direct-current (DC) conductance.

If dI represents a change in collector or drain current caused by a small change in base or gate voltage dE, then the transconductance is approximately:

$$g_m = dI / dE$$

As the size of the interval approaches zero -- that is, the change in base or gate voltage becomes smaller and smaller -- the value of dI / dE approaches the slope of a line tangent to the curve at a specific point. The slope of this line represents the theoretical transconductance of an FET for a given gate voltage and drain current.

4/14/03
http://whatis.techtarget.com/definition/0,,sid9_gci214200,00.html

The linear model of the MOSFET

The linear model describes the behavior of a MOSFET biased with a small drain-to-source voltage. As the name suggests, the MOSFET, as described by the linear model, acts as a linear device, more specifically a linear resistor whose resistance can be modulated by changing the gate-to-source voltage. In this regime, the MOSFET can be used as a switch for analog signals or as an analog multiplier.

The linear model for the drain current is:

$$I_D = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}, \text{for } |V_{DS}| << (V_{GS} - V_T) \qquad (7.3.6)$$

Note that the capacitance in the above equations is the gate oxide capacitance per unit area. Also note that the drain current is zero if the gate-to-source voltage is less than the threshold voltage. The linear model is only valid if the drain-to-source voltage is much smaller than the gate-to-source voltage minus the threshold voltage. This insures that the velocity, the electric field and the inversion layer charge density is indeed constant between the source and the drain.

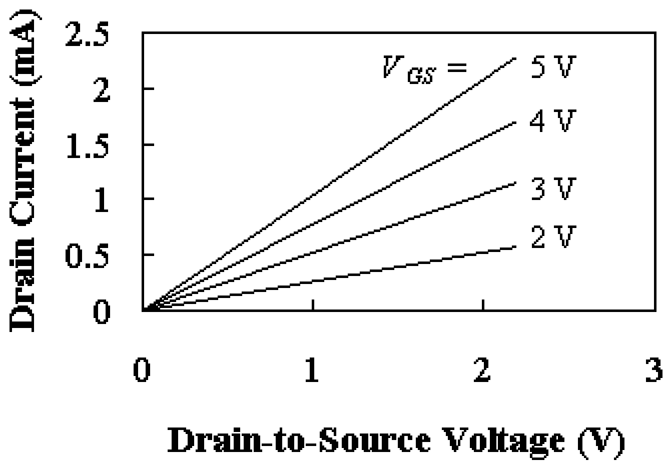

Figure 7.3.1 : Linear *I-V* characteristics of a MOSFET with V_T = 1 V. (μ_n = 300 cm^2/V-s, W/L = 5 and t_{ox} = 20 nm).

The figure illustrates the behavior of the device in the linear regime: While there is no drain current if the gate voltage is less than the threshold voltage, the current increases with gate voltage once it is larger than the threshold voltage. The slope of the curves equals the conductance of the device, which increases linearly with the applied gate voltage. The figure clearly illustrates the use of a MOSFET as a voltage-controlled resistor.

The quadratic model

The quadratic model uses the same assumptions as the linear model except that the inversion layer charge density is allowed to vary in the channel between the source and the drain.

The derivation is based on the fact that the current at each point in the channel is constant. The current can also be related to the local channel voltage.

Considering a small section within the device with width *dy* and channel voltage $V_C + V_S$ one can still use the linear model described by equation (7.3.6), yielding:

$$I_D = \mu C_{ox} \frac{W}{dy}(V_G - V_S - V_C - V_T)dV_C \quad (7.3.7)$$

where the drain-source voltage is replaced by the change in channel voltage over a distance *dy*, namely dV_C. Both sides of the equation can be integrated from the source to the drain, so that *y* varies from 0 to the gate length, *L*, and the channel voltage V_C varies from 0 to the drain-source voltage, V_{DS}.

$$\int_0^L I_D dy = \mu C_{ox} W \int_0^{V_{DS}} (V_G - V_S - V_C - V_T)dV_C \quad (7.3.8)$$

Using the fact that the DC drain current is constant throughout the device one obtains the following expression:

$$I_D = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}], \quad \text{for } V_{DS} < V_{GS} - V_T \quad (7.3.9)$$

The drain current first increases linearly with the applied drain-to-source voltage, but then reaches a maximum value. According to the above equation the current would even decrease and eventually become negative. The charge density at the drain end of the channel is zero at that maximum and changes sign as the drain current decreases. As explained in section 6.2, the change in the inversion layer does go to zero and reverses its sign as holes are accumulated at the interface. However, these holes cannot contribute to the drain current since the reversed-biased p-n diode between the drain and the substrate blocks any flow of holes into the drain. Instead the current reaches its maximum value and maintains that value for higher drain-to-source voltages. A depletion layer located at the drain end of the gate accommodates the additional drain-to-source voltage. This behavior is referred to as drain current saturation.

Drain current saturation therefore occurs when the drain-to-source voltage equals the gate-to-source voltage minus the threshold voltage. The value of the drain current is then given by the following equation:

$$I_{D,sat} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2}, \quad \text{for } V_{DS} > V_{GS} - V_T \quad (7.3.10)$$

The quadratic model explains the typical current-voltage characteristics of a MOSFET, which are normally plotted for different gate-to-source voltages. An example is shown in Figure 7.3.2. The saturation occurs to the right of the dotted line which is given by $I_D = \mu\, C_{ox}\, W/L\, V_{DS}^2$.

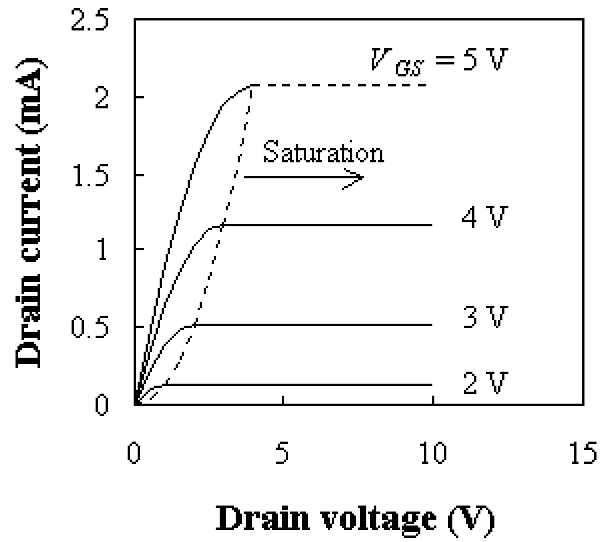

Figure 7.3.2: Current-Voltage characteristics of an n-type MOSFET as obtained with the quadratic model. The dotted line separates the quadratic region of operation on the left from the saturation region on the right.

The drain current is again zero if the gate voltage is less than the threshold voltage.

$$I_D = 0, \quad \text{for } V_{GS} < V_T \tag{7.3.11}$$

For negative drain-source voltages, the transistor is in the quadratic regime and is described by equation (7.3.9). However, it is possible to forward bias the drain-bulk p-n junction. A complete circuit model should therefore also include the p-n diodes between the source, the drain and the substrate.

The quadratic model can be used to calculate some of the small signal parameters, namely the transconductance, g_m and the output conductance, g_d.

The transconductance quantifies the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant, or:

$$g_m \stackrel{\Delta}{=} \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} \tag{7.3.12}$$

The transconductance in the quadratic and linear regions is given by:

$$g_{m,quad} = \mu C_{ox} \frac{W}{L} V_{DS} \tag{7.3.13}$$

which is proportional to the drain-source voltage for $V_{DS} < V_{GS} - V_T$. In saturation, the transconductance is constant and equals:

$$g_{m,sat} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) \tag{7.3.14}$$

The output conductance quantifies the drain current variation with a drain-source voltage variation while keeping the gate-source voltage constant, or:

$$g_d \stackrel{\Delta}{=} \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}} \quad (7.3.15)$$

The output conductance in the quadratic region decreases with increasing drain-source voltage:

$$g_{d,quad} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T - V_{DS}) \quad (7.3.16)$$

and becomes zero as the device is operated in the saturated region:

$$g_{d,sat} = 0 \quad (7.3.17)$$

Example 7.1	Calculate the drain current of a silicon nMOSFET with V_T = 1 V, W = 10 μm, L = 1 μm and t_{ox} = 20 nm. The device is biased with V_{GS} = 3 V and V_{DS} = 5 V. Use the quadratic model, a surface mobility of 300 cm^2/V-s and set V_{BS} = 0 V. Also calculate the transconductance at V_{GS} = 3 V and V_{DS} = 5 V and compare it to the output conductance at V_{GS} = 3 V and V_{DS} = 0 V.
Solution	The MOSFET is biased in saturation since $V_{DS} > V_{GS} - V_T$. Therefore the drain current equals: $$I_D = \mu_n C_{ox} \frac{W}{L}\frac{(V_{GS} - V_T)^2}{2} = 300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times \frac{(3-1)^2}{2} = 1.04 \text{ mA}$$ The transconductance equals: $$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T) = 300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times (3-1) = 1.04 \text{ mS}$$ and the output conductance equals: $$g_d = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T - V_{DS}) = 300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times (3-1-0) = 1.04 \text{ mS}$$

The measured drain current in saturation is not constant as predicted by the quadratic model. Instead it increases with drain-source voltage due to channel length modulation, drain induced barrier lowering or two-dimensional field distributions, as discussed in section 7.7.1. A simple empirical model, which considers these effects, is given by:

$$I_{D,sat} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS}), \quad \text{for } V_{DS} > V_{GS} - V_T \tag{7.3.18}$$

Where λ is a fitting parameter.

Taken from Principles of Semiconductor Devices by Bart Van Zeghbroeck
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http://ece-www.colorado.edu/~bart/book/book/chapter7/ch7_3.htm