ECEn452 Winter 2004
Week 4
Background Reading

Wet Etching
Read pages 426-431 from Sze before beginning this lab

10.2.3 Total Contact Resistance

The value of total contact resistance R_T required in an integrated circuit varies with the specific device but is generally in the 10–100 Ω range. The R_c value that can be tolerated varies from 10^{-6} Ω-cm^2 to about 10^{-5} Ω-cm^2. Of concern as devices continue to decrease in size is how contact resistance must scale in order to not degrade the device. Bipolar behavior seems to dictate that the current density of emitters remain near 400 A/cm^2 regardless of emitter area. Since allowable circuit voltage drops will remain constant, independent of current and geometry, as the current decreases, the resistance can increase commensurately. Thus, the move to smaller bipolar geometries should not put additional restraints on contact resistance. In MOS circuits, however, reduced geometries may lead to reduced voltages as well as currents. In such cases, a constant resistance value during size reduction may be required, and that must come from a reduction of the contact resistance r_c.

To see how R_c and bulk resistivity ρ interact, consider Fig. 10.9. It has curves of contact resistance versus contact area for representative values of R_c and curves of spreading resistance versus area for different silicon doping levels. These curves show that for the total resistance to be in the <100 Ω range for the small-diameter contacts, the silicon doping must be 0.01 Ω-cm or less. The heavy doping is required for r_s as well as for R_c reduction. Current technology primarily uses locally diffused regions (p^+ or n^+) under the contact to secure the high doping necessary. However, the doping that occurs during regrowth from a metal-alloyed region can also be used. For example, regrowth from aluminum will give p-type aluminum-doped silicon, as will regrowth from gold to which small

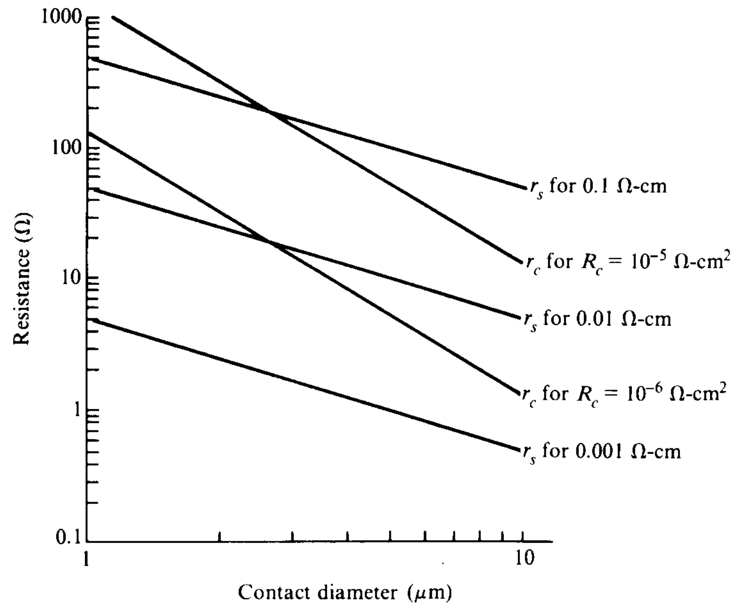


FIGURE 10.9

Spreading resistance of circular contacts for various resistivities of material and contact resistance for two values of specific contact resistance.

FIGURE 1C

Specific cor sus total co various she values.

amounts of gallium have been added. Similarly, gold with small amounts of antimony will regrow an antimony-doped n-region. Sandblasting has also been used to provide a damaged surface layer whose electrical properties are similar to those of heavily doped surfaces.

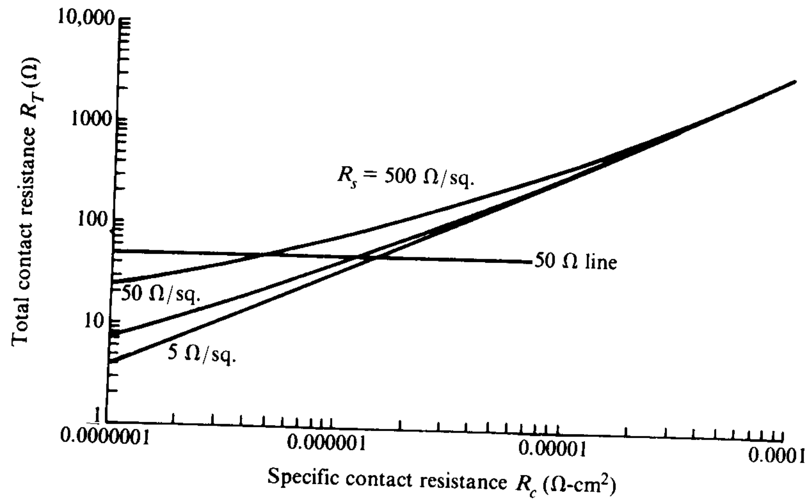
Perhaps more directly applicable to the understanding of these relations as they pertain to integrated circuits is a reconsideration of Fig. 10.3, which showed contact to a thin isolated diffused layer. The total contact resistance R_T for that geometry can be approximated by Eq. 10.5. Using that same equation, R_T versus specific contact resistance is plotted for representative sheet resistances of 5, 50, and 500 Ω/sq. and shown in Fig. 10.10. For example, with a contact 1 μm long by 3 μm wide, a contact resistance of less than 50 Ω can, for any of the three sheet resistance values shown, only be achieved if R_c is less than about 10^{-6} Ω-cm². However, with a 5 μm contact, 50 Ω can be obtained with a 5 Ω/sq. sheet and an R_c of just a little less than 10^{-5} Ω-cm². For this reason, as contacts have shrunk, more emphasis has been placed on reducing specific contact resistance.

10.2.4 The Aluminum–Silicon Ohmic Contact

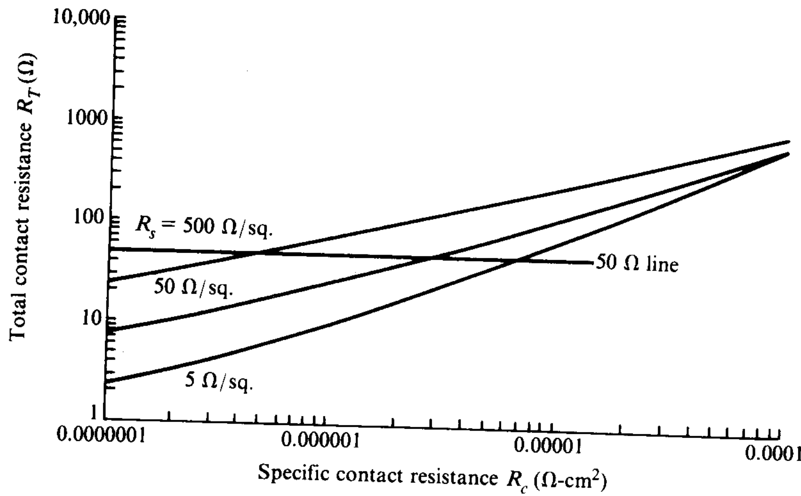
Silicon has an appreciable solubility at elevated temperatures in several of the possible contact materials. Aluminum, which has been used since the inception of the planar silicon IC for contacts and metallization, is an example. Its ability to dissolve thin layers of

FIGURE 10.10

Specific contact resistance versus total contact resistance for various sheet resistance values.



(a) 1 μm long by 3 μm wide contact



(b) 5 μm long by 3 μm wide contact

SiO_2 helps ensure good physical contact to the silicon even if surface cleaning is not complete. However, enough silicon will dissolve in the aluminum during the contacting operation to form pits in the silicon surface. The pits are filled with aluminum, and the phenomenon is often referred to as aluminum spiking. Fig. 10.11 shows the way the dissolution (alloying) takes place. This pitting is seen well below the aluminum–silicon eutectic temperature of 577°C. (See Appendix B for a discussion of solubility, eutectic temperature, and phase diagrams.) Some early work postulated that the eutectic tem-

perature was depressed because of stress and that melting actually occurred. However, the high diffusivity of silicon in aluminum can account for the observed effect.

Like aqueous etching, the etching of silicon by metals is crystallographic orientation dependent, and as in aqueous etching, the slow etching planes are the {111}'s (10). Because of the slow dissolving (111)'s, it is possible to get very flat alloy fronts when alloying into (111) surfaces (11). Thus, germanium and silicon alloy transistors were all made in (111) oriented wafers. The equilibrium form of patterns formed by the aluminum–silicon interaction will appear as flat-bottomed, triangular pits in (111) and square-topped, pyramidal pits in (100) material. Occasionally, hexagonal shapes will be seen on (111) material because at early stages the $(\bar{1}11)$, $(1\bar{1}1)$, and $(11\bar{1})$ planes as well as the $(\bar{1}\bar{1}1)$, $(1\bar{1}\bar{1})$, and $(\bar{1}1\bar{1})$ planes limit the reaction.[3] In cross section, they will appear as in Fig. 10.11. Since no (111) plane is parallel to a (100) surface to act as an etch stop, the aluminum–silicon interface of contacts on (100) wafers will not be smooth. Of more importance, because the thin layer of interfacial oxide that must first be dissolved will not fail uniformly, different regions will begin reacting at different times. The first ones can allow enough silicon into the aluminum to saturate much of the contact

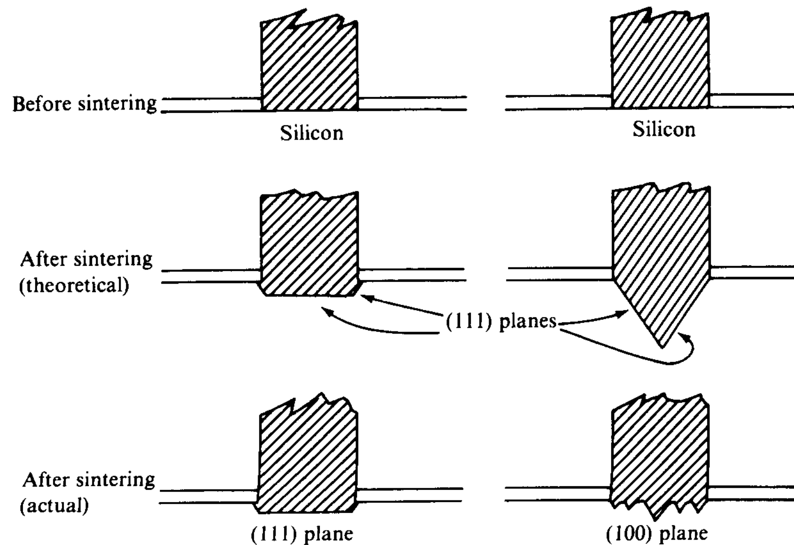


FIGURE 10.11

Metal front before and after sintering (alloying). (The actual depth depends on sinter time, temperature, and amount of metal present.)

[3] It is arguable that the equilibrium shapes formed by solid-state diffusion might be different from those occurring during liquid dissolution, but experimentally, they are observed to be the same.

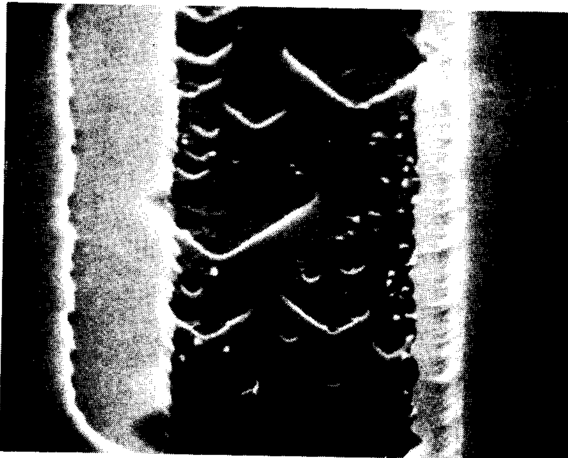
and thus limit dissolution over the remainder of the contact area. The unfortunate result is that the first pits will be much deeper than the rest and, in shallow junction devices, may extend through a junction and cause shorting. Fig. 10.12 shows scanning electron microscope photographs of (111) and (100) silicon surfaces after the aluminum contacts have been removed. The excessive pitting of the (100) surface is clearly visible.

A planar transistor or an integrated circuit has rather thin metallization, and the sintering temperature is intentionally held below the metal–silicon eutectic. Nevertheless, the solubility of silicon in aluminum is high enough for appreciable dissolution to occur (12–18). The total amount of silicon dissolved can be calculated from the

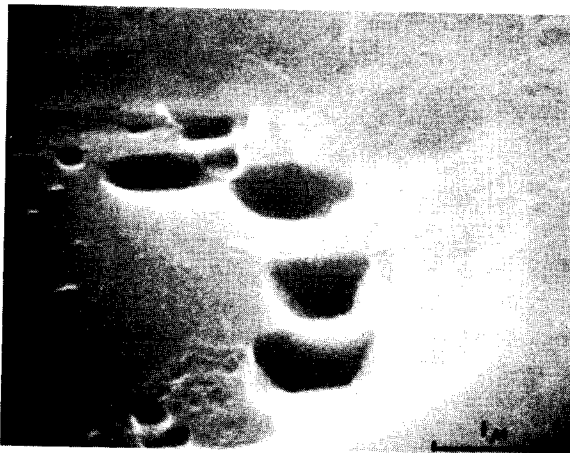
RE 10.12

iews of (111) and (100) surfaces showing pits ing after removing alu- metallization from con- ndows.

: Photographs courtesy of . Ghate, Texas Instru- ncorporated.)



(a) (111) plane



(b) (100) plane

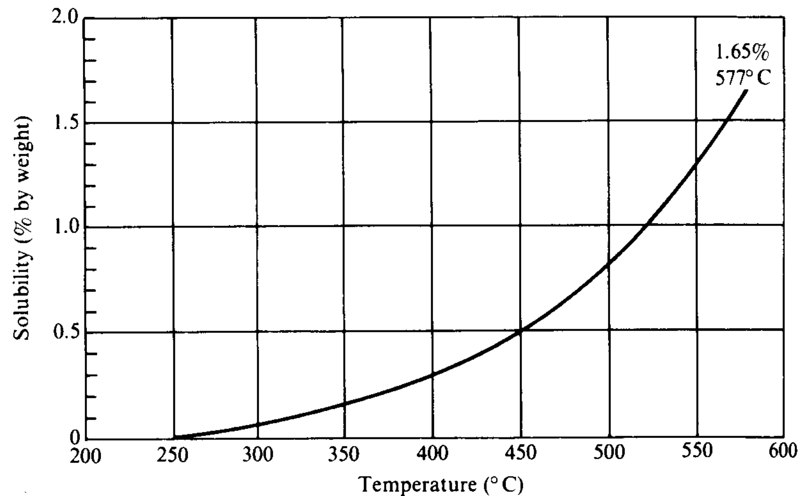


FIGURE 10.13

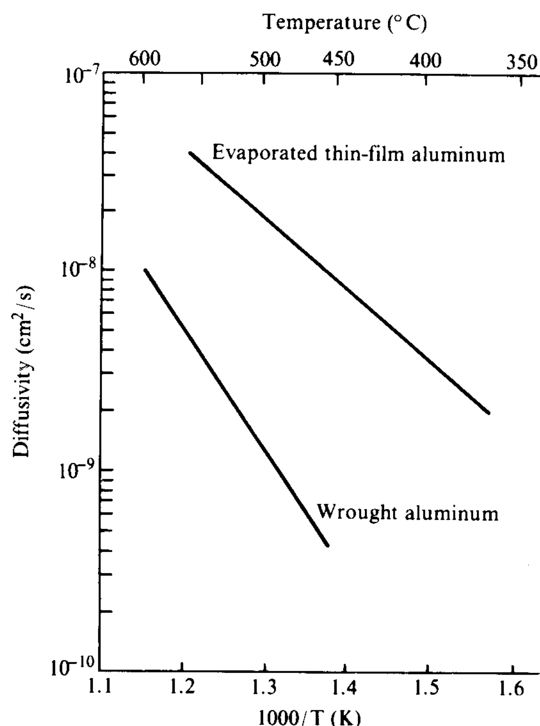
Solubility of silicon in aluminum. (*Source:* From data in Max Hansen, *Constitution of Binary Alloys*, McGraw-Hill Book Co., New York, 1958.)

solid solubility of silicon in aluminum and the amount of aluminum available. Fig. 10.13 gives solubility data up to 577°C. Determining the amount of solvent aluminum is not completely straightforward, however. In principle, given enough time for the silicon to diffuse along its length, the entire aluminum lead system could become saturated. In practice, the time at high temperature is not enough for this to happen. Substantial diffusion distances are possible, however, because of the high silicon diffusivity (Fig. 10.14). The effect of leads acting as silicon sinks can clearly be seen by noting that when a contact has a lead extending out from it in one direction only, more dissolution generally occurs on that side of the contact. Since the removal of the silicon does not produce a void under the aluminum, it must be assumed that a simultaneous motion of the aluminum occurs (aluminum self-diffusion) that keeps voids from forming. In order to use the data of Fig. 10.14, it must be further assumed that it is the silicon diffusion, and not that of aluminum, that limits motion of silicon in the aluminum.

EXAMPLE ☐ If an aluminum lead the same width as the contact (10 μm) and 1 μm thick extends out from the contact to infinity in one direction only, how much silicon will diffuse into it in 20 minutes at 450°C? Assume that the aluminum over the contact is already saturated with aluminum and that it will remain saturated by diffusion from the wafer.

FIGURE 10.14

Diffusivity of silicon in aluminum. (The upper curve is representive of IC metallization; the lower curve for wrought aluminum is intended only as a trend line. The spread of reported data is substantial.) (*Source:* Upper curve data from J.O. McCaldin and H. Sankur, *Appl. Phys. Lett. 19*, p. 524, 1971; lower curve based on old data tabulated in McCaldin and Sankur.)



From Fig. 10.13, at 450°C, the solubility limit of silicon in aluminum is ~0.5% by weight, or 0.014 gram/cc. Let that equal N_0. $N(x) = N_0 \operatorname{erfc}(x/2\sqrt{Dt})$. (For details on diffusion, see Chapter 8.) The total amount M of silicon that diffused in is given by $\int_0^\infty N(x)dx$, or

$$M = \int_0^\infty \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) = 2N_0\sqrt{\frac{Dt}{\pi}}$$

From Fig. 10.14, at 450°C, $D \cong 10^{-8}$ cm²/s. Substituting these numbers into the equation above gives $M = 5.5 \times 10^{-5}$ grams/cm². The cross section of the lead is 10^{-7} cm², so 5.5×10^{-12} grams of silicon diffused down the lead. Since silicon has a density of 2.3 grams/cc, this represents a volume of $\sim 2.4 \times 10^{-12}$ cc. If the contact were square, its area would be 10^{-6} cm²; if the silicon were uniformly removed from beneath it, the surface would move down 2×10^{-7} cm. While this number may seem very small, if all the silicon came from one 3 μm square area, as might happen in a (100) wafer, the pit would be 0.8 μm deep. □

Experimentally,[4] it has been reported that sintering at 300°C produces discernible pitting with some depths to 0.2 μm. At 350°C, pits of 0.75 μm have been observed, and at 450°C, pits of 2 μm (19). Individual behavior will, of course, depend on the amount and placement of the aluminum over and around the contact window.

In order to prevent such pitting, the aluminum may be deposited saturated with silicon so that it is unable to absorb any more (12, 13, 20), or it may be deposited over a thin sacrificial layer of polycrystalline silicon (21). When this problem was first recognized, there was considerable reticence to the use of silicon-doped aluminum because of the difficulty of deposition. A number of other alternatives, such as the deposition of a thin layer of aluminum followed by sintering and then a subsequent thick aluminum deposition, were also tried (18). With the later development of improved sputtering equipment came the routine deposition of aluminum–silicon of controlled composition.[5] However, oxide radiation damage may be induced that requires additional thermal annealing for removal.

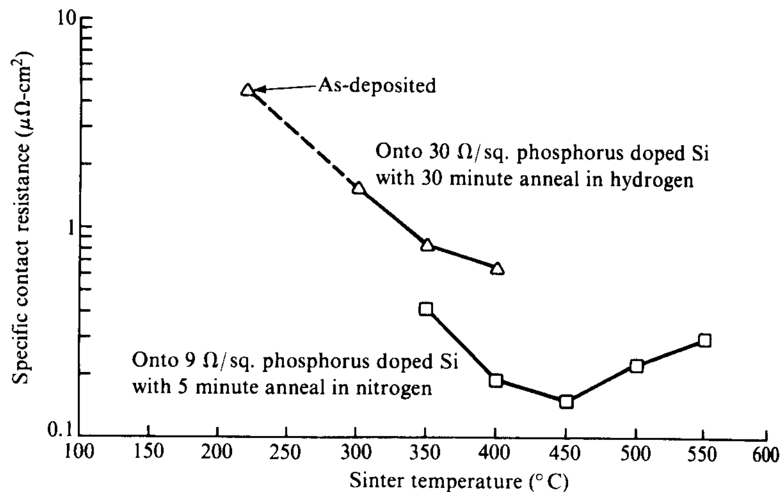


FIGURE 10.15

Specific contact resistance versus sinter temperature of aluminum on heavily doped phosphorus-diffused silicon. (The two sets of data were obtained from two different test patterns that may not give comparable results.) (*Source:* Upper curve data from R.A. Levy et al., *J. Electrochem. Soc. 132*, p. 159, 1985; lower curve calculated from data in H.M. Naguib and L.H. Hobbs, *J. Electrochem. Soc. 124*, p. 573, 1977.)

[4]Some idea of the penetration depth can be obtained from cross sections, but it is difficult to find a section that stops just at the bottom of a pit. Referenced data were obtained by replicating the contact surface after etching away the aluminum and examining the replica with a SEM.

[5]The addition of silicon requires some modification of the procedures used to bond connecting wires to the chip bonding pads. Because of the silicon precipitates, somewhat different etching techniques are needed to prevent silicon from being left on the wafer surface after lead pattern definition and to prevent jagged edge definition.

FIGURE 10.1
Aluminum res
temperature v
silicon present
data in L.W. K
of Aluminum–S
Taylor Lyman,
book, American
als, 1948.)

10.2.5 The S
Silicon Ohmi

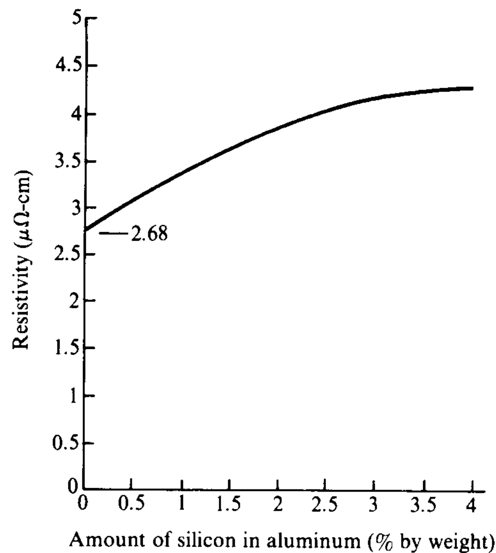


FIGURE 10.16

Aluminum resistivity at room temperature versus amount of silicon present. (*Source:* From data in L.W. Kempf, "Properties of Aluminum–Silicon Alloys," in Taylor Lyman, ed., *Metals Handbook,* American Society for Metals, 1948.)

To assess the minimum temperature that can be used for sintering, and thus to reduce pitting, several studies of specific contact resistance versus sinter temperature have been made (19, 22, 23). Fig. 10.15 shows the general behavior for n-type silicon and illustrates the need for sinter temperatures in the 400°C–450°C range. The reason for the upturn near 450°C for n-type silicon is not due to an increase in the bulk resistance of aluminum because of increased silicon uptake since, as shown in Fig. 10.16, the effect of silicon is considerably less than that of the sintering. The increase, not observed in p-type, apparently occurs because enough aluminum-doped silicon (p-type) regrows in the contact window to affect the contact resistance.

10.2.5 The Silicide–Silicon Ohmic Contact

One of the requirements of contact materials is that they withstand heating to a few hundred degrees while in contact with the silicon. Often, such heating is required for breaking through the residual surface oxide so that good electrical contact can be made. In addition, annealing near 500°C is sometimes required to adjust the SiO_2–Si interface states, and in multilevel metal systems, the interlevel insulator may require a 300°C–500°C deposition temperature. The result is that many potential metal–silicon contacts cannot exist because the silicon and the metal react to form a silicide. However, the silicides generally have very high electrical conductivity and in