ECEn 452 – Semiconductor Devices Lab

Week 4: "Wet Etching/Annealing"

Objectives

Introduction

This lab is designed to apply the basics of wet etching and metal annealing.
Wet Etching: You will learn about the relationships between temperature and etch rate and will have the opportunity to see how different metals respond to etching. You will also see how well the metals you evaporated in Week 2 adhere to silicon.
Metal Annealing: After the deposition of metal onto a semiconductor surface and creating a pattern, an annealing step is typically done. Placing a wafer into a high temperature furnace for a given amount of time, usually with a specific gas environment inside the furnace, does this. The purpose of the anneal is to decrease the contact resistance between the metal and the semiconductor by causing a small amount of metal and semiconductor to go into "solution" and intermix. Annealing also can help to increase the adhesion of the metal to the semiconductor. When designing a process recipe for annealing, usually you want to obtain the lowest contact resistance possible. The parameters you have to work with to obtain this are anneal temperature and anneal time. Your choices for temperature are from room temperature all the way up to 1200°C. For annealing time you are limited only by how fast the insertion rod can move in and out of the furnace.

Prelab Questions

1. What effect does temperature have on etch rate in a chemical etch?
2. Draw a side view diagram of an isotropic chemical etch profile if a) the photoresist mask adheres well to the layer being etched b) the photoresist mask does not adhere well to the layer being etched.
3. What is the optimal anneal time, temperature, and atmosphere for aluminum on silicon according the graphs found in your background reading?
4. What would be the effects of annealing a metal on a semiconductor for a long time at high temperatures? Why is this not necessarily the best way to produce a low resistance contact?

Objectives

The following objectives will need to be completed in order. The first group in a particular day needs to move at a steady pace so that the group behind them does not overlap them in the use of any equipment – although both groups will likely be sharing the annealing furnace by the end of the day.

1. TLM Pattern on Metallized Wafers:

   Using the TLM pattern mask specifically created for this laboratory, use photolithography to transfer this pattern onto a wafer coated with Aluminum and a wafer coated with Nickel (the coating was done in Week 2). This mask was created using a high resolution printer and a transparency so the edges will look a lot rougher than the features you looked at last week on the e-beam written photomasks. Use your optimal recipes for photolithography developed in Week 3. After pattern development, you should also include a "hard bake" step. This hard bake step is done on a hot plate at 110°C for 60 seconds. A hard bake is used to harden up the resist and make it adhere better to the layer below.

2. Metal Etching:

Essentially etching will take place by immersing a wafer coated with metal into an etch solution. Before you do this with a patterned wafer however, you need to find out about some of the characteristics of each metal etch (aluminum and nickel) –most importantly the etch rate as a function of temperature. Read the MSDS on the aluminum and nickel etchants you will be using and read the labels on their containers carefully. What is in each of the etchants? Determine an optimal etch temperature for both the aluminum and the nickel etchant. For the Aluminum etchant, program the hot bath for the temperature you have chosen, for the nickel etchant if you want to heat it up, place a glass dish containing the etchant on a hot plate and use a thermometer to monitor its temperature. Place the 4" wafers you patterned in step 1 into the etchant for the correct amount of time based on published etch rates. Then remove your wafers and rinse them thoroughly in deionized water for at least 60 seconds. Examine the patterns under a microscope to make sure all the metal was etched away. (This should be fairly obvious even without the microscope because the semiconductor will look much darker than the metal). When you are satisfied, remove the resist from your wafer using the solvent chemical cleans learned in Week 3. If you didn't etch far enough, put the wafers back in the etchant. How accurate were the published etch rates for the etchants based on your 100 nm thick samples?

3. Over etching:

Over etching typically occurs when a sample is left in an etchant too long and the etchant begins to undercut the photoresist mask significantly. After etching but before removing the photoresist, examine the pattern under the microscope. Undercutting should lead to a rounding of sharp features in the metal as well as a line shifted in from the original photoresist outline indicating the edge of the metal features. Record all of your observations in your lab notebook. Note: If metal is too thin, over etching may be difficult to see. Why is this the case?

4. Metal Adhesion:

One of the things we should be worried about when depositing and patterning metal on a semiconductor is how well the metal sticks to the wafer underneath. One of the first ways developed to test this was the "Scotch tape test." There are now more sophisticated ways to test metal adhesion, but the scotch tape test is still used. To do this test, take a piece of scotch tape and place the sticky side over some of your patterned metal features (this can only be done after Objectives 2 and 3). Only use a few features on the very edge of your wafer. Pull off the scotch tape and see if the metal stuck to the tape or the wafer. Try it for both the aluminum and nickel samples. This is the type of quick "go or no go" test that is still very handy.

5. Wafer Cleaving:

Have a supervisor demonstrate the correct procedure for cleaving silicon wafers (the nick and press method – due not drag the cleaving scribe across the wafer surface). When you are confident in your cleaving skills, cleave your wafers that you patterned in Objective 2. Cleave the wafers so that you are left with fairly large samples (~ 1 inch x 1 inch) that contain the TLM patterns we are interested in – make sure you have at least 6 of these cleaved samples.

6. Tube Furnaces:

Tube furnaces are an important part of high temperature silicon processes—used for annealing, oxide growth, diffusion, etc. Have a supervisor show you the main features of the tube furnace contained in the clean room including the gas intake system, the sliding insert arm, and the electronic controller. Have the supervisor demonstrate programming the controller for temperature, arm speed, and gas flow. Record in your lab notebooks the general processing for programming and running the furnace.

7. Metal Annealing:

Pick annealing parameters to produce 6 different annealing processes, keep an "as deposited" sample as an experimental control. Vary the temperature and time for your aluminum and nickel samples to be able to observe effects of under, over, and optimal annealing. (Remember that temperature has the largest effect on the contact resistance.) Anneal one of the small nickel and aluminum pieces cleaved in STEP 5 for each of the annealing settings you decide on. Keep track of what treatment was done to each of the pieces because you will be testing these effects in next week's lab.

8. Annealing Surface Effects:

After each annealing step completed in Objective 7, examine the metal samples under a microscope. Can you see the differences between the under, over, and optimal annealing? Is it what you expected? Has the surface changed significantly? Can you see evidence of the metal and semiconductor forming a solution? Are there differences in the aluminum versus the nickel samples? Record your visual observations in your lab book. Also try the "scotch tape test" to see if the adhesion has changed at all due to the annealing.

If time is running late for your lab session and you still need to anneal more samples, you can finish some of them up during next week's lab session. During that session you will be testing contact resistance of you metal/semiconductor interface but if need be some members of you lab group could anneal further samples while others did testing.