ECEn 452 – Semiconductor Devices Lab

Week 9: “The Gate”

Objectives

Introduction

In the previous lab, you etched source and drain features into the oxide of your wafers and diffused in a dopant (Figure 1). The next step in the MOSFET process is to add the gate region. Mask alignment will be used in order to correctly place the gate region over each individual source and drain. The difference between a functional and non-functional chip could come down to the quality of the alignment. In this lab, you will prepare your wafers for another lithography step and then use the aligner to align the gate mask over the wafer, using UV light to expose the photoresist. Alignment tolerance is how close you can come to perfect alignment. The developed photoresist should expose the field oxide between the two n^+ regions. This will be etched in the BOE. You should produce four wafers that have holes etched into the field oxide layer. The etched region between the n^+ regions will define the “gate oxide” area. If all goes well the MOSFET should look like Figure 2. After this you will then grow another oxide over the surface of your wafer that will serve as the gate oxide.

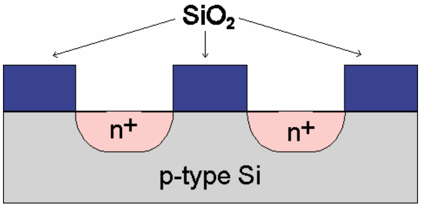


Figure 1

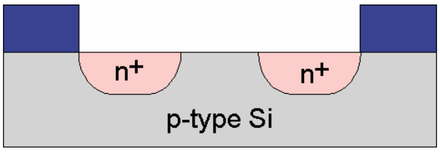
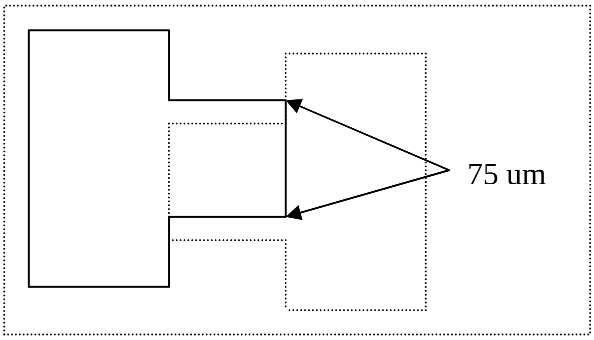


Figure 2

Prelab Questions

1. If you’re looking at the left side of the wafer and it looks aligned but the rotation is actually off by 1 degree, how far off is the alignment on the right side of the wafer 3 inches away?
2. Using the techniques of the last problem, how much can our rotation angle be off if we need to stay within 50 um of horizontal 3 inches away?
3. In the figure below, you are to align the mask feature on the left with the feature already on the wafer on the right. You must have 90% vertical overlap for the feature to function properly. How many microns can you be off in the alignment?



4. Using what you learned in Lab 6, what are the ideal growth conditions for 1000 Angstroms of silicon dioxide?

Objectives

This lab has a set procedure that must be performed in the proper sequence.

1. Photoresist Application:

Using your standard lithography process, apply photoresist to the 4 MOSFET process wafers. (Be sure to dehydration bake!)

2. Mask Alignment:

Using the Karl Suss aligner, align the “Gate” mask to the existing source and drain patterns on your wafers. Remember to first line your microscope up on the mask’s alignment marks on either side of the wafer. Then position your wafer under these alignment marks. (The procedure will be the same that you learned in Week 7 with the dielectric picture). Let everyone in your group do some alignment. Align and expose all 4 process wafers, and then develop the pattern.

3. Alignment Tolerance:

Using an optical microscope, estimate the alignment tolerance for the wafers. You might notice that some areas look aligned while others do not. This is an indication of poor alignment. Map your alignment tolerance over the entire wafer surface and document it. If the alignment tolerance is too poor, strip off the photoresist and repeat the lithography steps. Consult the lab supervisor as to what would be “too poor.”

4. Plasma Etching – Descum:

When you are satisfied with the alignment of your wafer, descum it for about 15 seconds in the oxygen plasma. This will remove thin films of photoresist that may have been left by the developer.

5. Oxide Etching:

Silicon dioxide etching is done using BOE (buffered oxide etch, or buffered HF). Because HF is dangerous, you need to be very careful during this processing step. BOE accurately etches thermally grown silicon dioxide at 100 nm per minute, but does not etch silicon. It is pretty easy to determine when BOE has etched through an oxide layer to an underlying silicon layer, because the silicon layer will appear dry when withdrawn from the BOE. If oxide still remains on the surface, a wafer will appear wet. Try using this technique to determine when you have finished etching through the oxide layer. If the exposed Si areas are too small, you may not see the “dry” appearance so observe the largest features available. Based on the known oxide etch rate, estimate the thickness of the oxide layer. This will likely be different from the original field oxide thickness that you grew because of the application and then removal of the spin-on-glass dopant layer. Verify using the optical microscope that you have etched all the way through the oxide.

6. Plasma Etching – Bulk PR Removal:

Use the Solitec Spinner to remove the photoresist on the silicon wafers. Inspect the wafers under the microscope to insure that all the photoresist has been removed.

7. Gate Oxide Growth:

On each of your 4 MOSFET processing wafers grow a 1000 Angstrom oxide using conditions calculated previously. (Before growing your oxide, strip any native oxide from your wafers by dipping them **briefly** in Buffered HF. Make sure the Buffered HF is very clean because the interface between the silicon and the gate oxide is very critical). Measure the thickness of the new field oxide using the ellipsometer or the nanospec after your gate oxide growth.