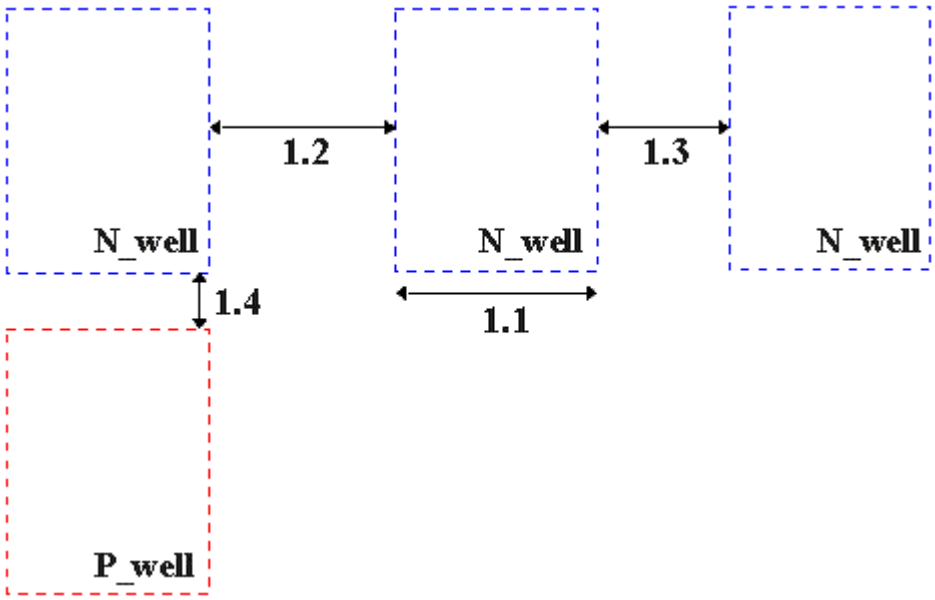
SCMOS Layout Rules - Well

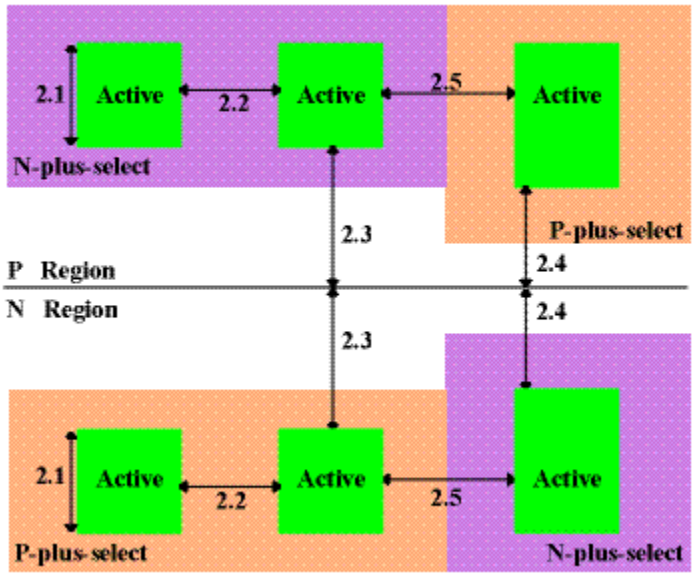
Rule	Description	SUBM	
		Lambda	Microns
1.1	Minimum width	12	3.6
1.2	Minimum spacing between wells at different potential	18	5.4
1.3	Minimum spacing between wells at same potential	6	1.8
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0



SCMOS Layout Rules - Active

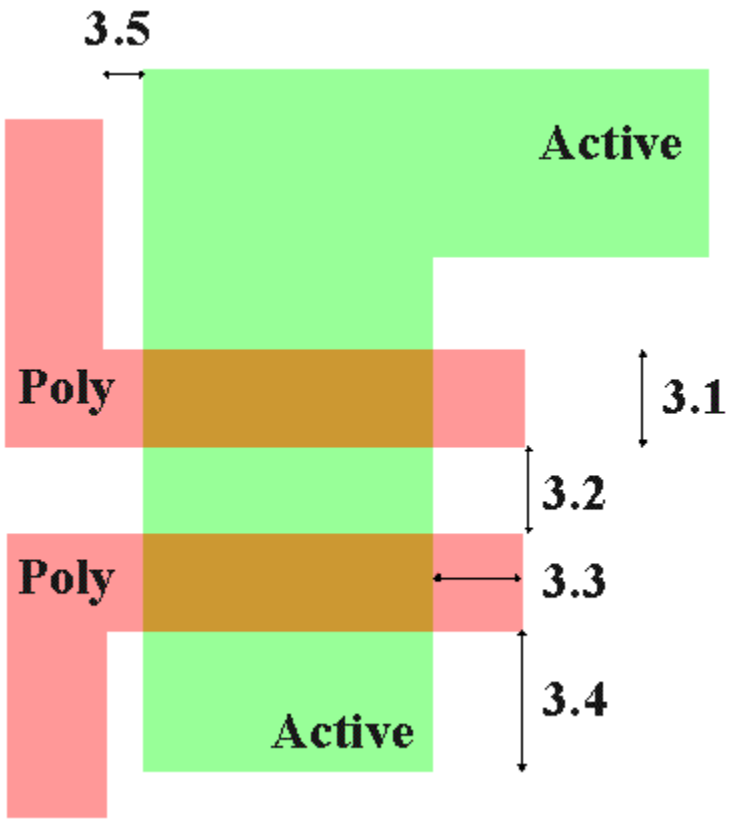
Rule	Description	SUBM	
		Lambda	Microns
2.1	Minimum width	3	0.9
2.2	Minimum spacing	3	0.9
2.3	Source/drain active to well edge	6	1.8
2.4	Substrate/well contact active to well edge	3	0.9
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	1.2

Note: For analog and critical digital designs, MOSIS recommends the minimum MOS *channel widths* (active under poly) to be 10 lambda i.e. 3 microns for submission to AMI ABN (1.5 micron process) and C5N (0.5 micron process).



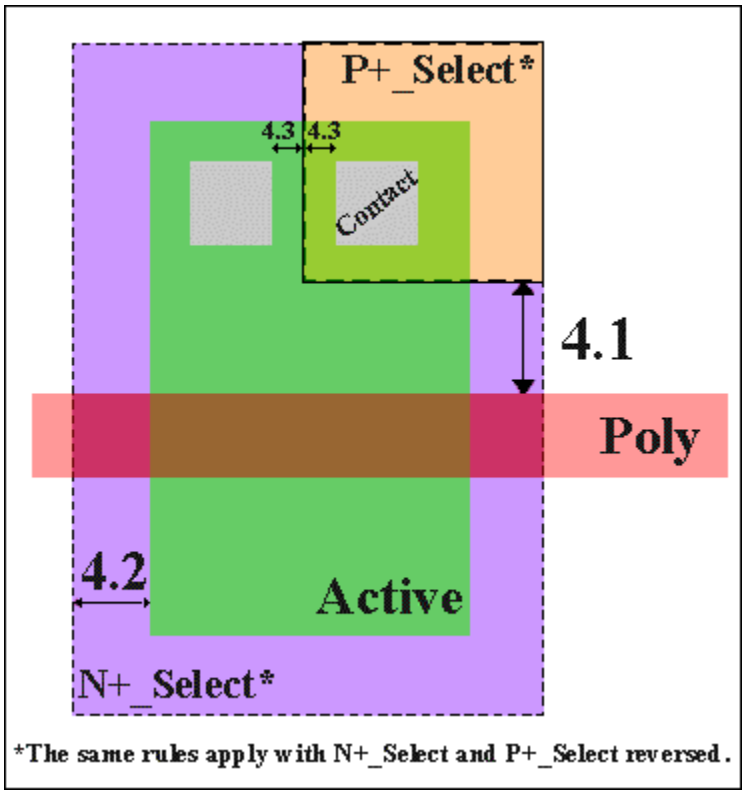
SCMOS Layout Rules - Poly

Rule	Description	SUBM	
		Lambda	Microns
3.1	Minimum width	2	0.6
3.2	Minimum spacing over field	3	0.9
3.3	Minimum gate extension of active	2	0.6
3.4	Minimum active extension of poly	3	0.9
3.5	Minimum field poly to active	1	0.3



SCMOS Layout Rules - Select

Rule	Description	SUBM	
		SUBM	Microns
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	0.9
4.2	Minimum select overlap of active	2	0.6
4.3	Minimum select overlap of contact	1	0.3
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	0.6



SCMOS Layout Rules - Contact to Poly

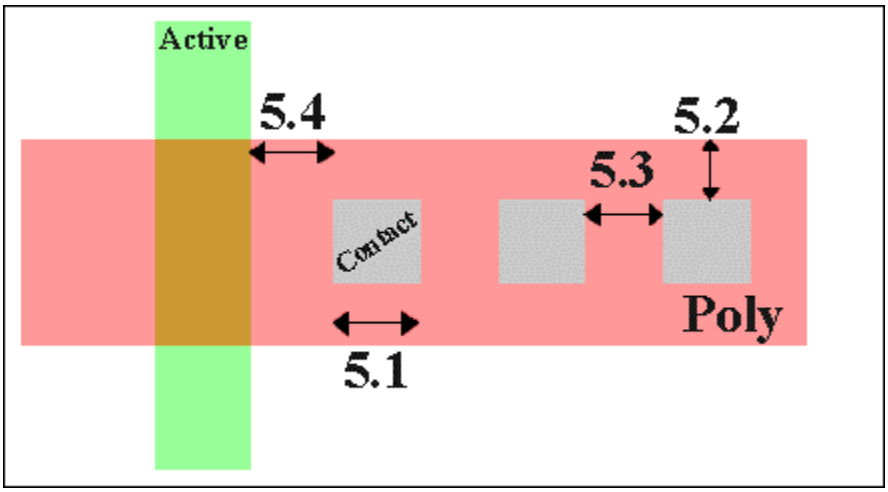
On 0.50 micron process (and all finer feature size processes), it is required that all features on the insulator layers (CONTACT, VIA, VIA2) must be of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

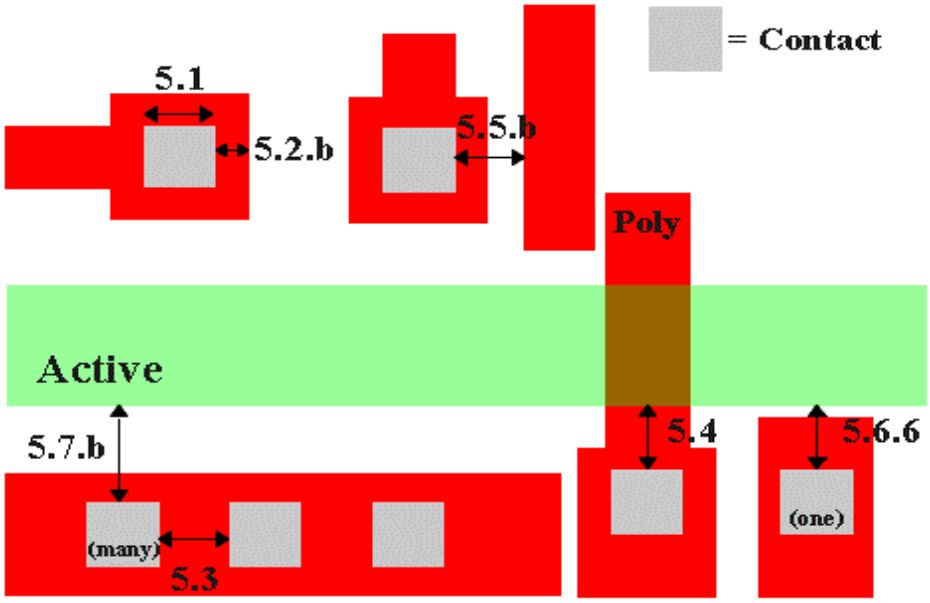
Since we want to avoid half lambda spacing rules (contact overlap in 5.2) we use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 5.1, 5.3, and 5.4, still apply and are unchanged.

Simple Contact to Poly

Rule	Description	SUBM	
		SUBM	Microns
5.1	Exact contact size	2x2	0.6x0.6
5.3	Minimum contact spacing	3	0.9
5.4	Minimum spacing to gate of transistor	2	0.6
5.2.b	Minimum poly overlap	1	0.3
5.5.b	Minimum spacing to other poly	5	1.5
5.6.b	Minimum spacing to active (one contact)	2	0.6
5.7.b	Minimum spacing to active (many contacts)	3	0.9

Note: Rule 5.2 is disabled, instead 5.2b, 5.5b, 5.6b, 5.7b are enabled in addition to rules 5.1, 5.3, 5.4





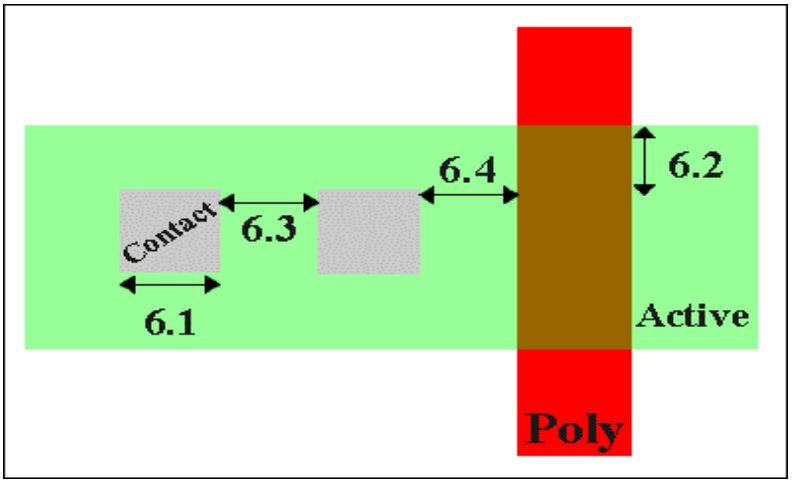
SCMOS Layout Rules - Contact to Active

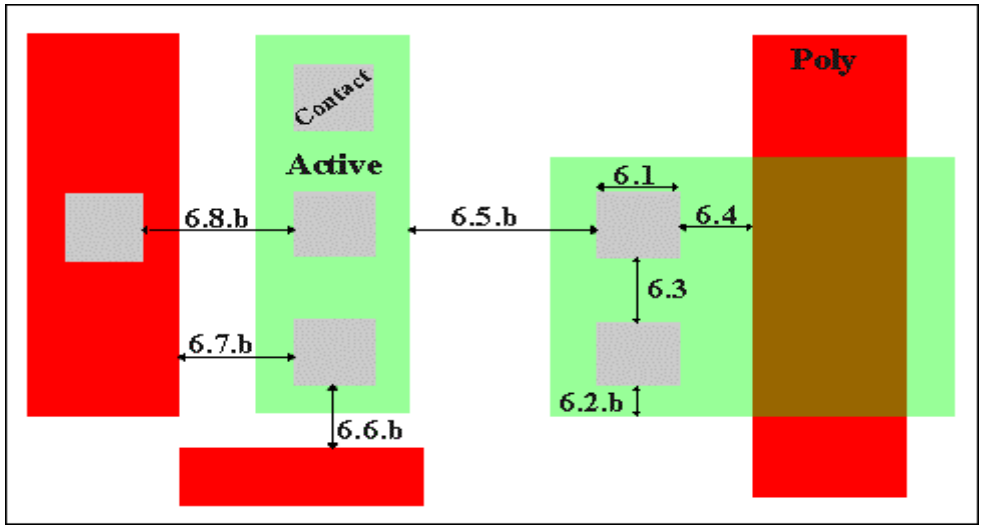
Simple
Contact to Active

Rule	Description	SUBM	
		Lambda	Microns
6.1	Exact contact size	2x2	0.6x0.6
6.3	Minimum contact spacing	3	0.9
6.4	Minimum spacing to gate of transistor	2	0.6
6.2.b	Minimum active overlap	1	0.3
6.5.b	Minimum spacing to diffusion active	5	1.5
6.6.b	Minimum spacing to field poly (one contact)	2	0.6
6.7.b	Minimum spacing to field poly (many contacts)	3	0.9
6.8.b	Minimum spacing to poly contact	4	1.2

If your design cannot handle the 1.5 lambda contact overlap in 6.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 6.1, 6.3, and 6.4, still apply and are unchanged. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

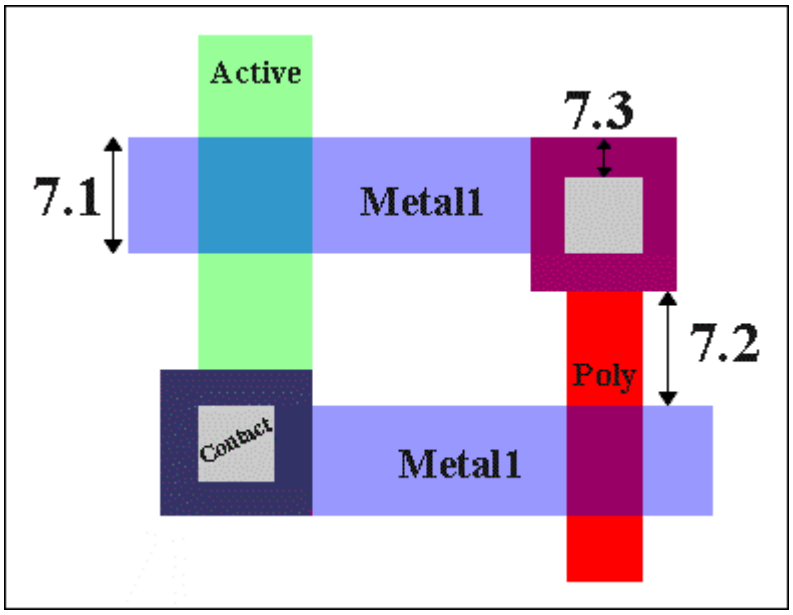
Note: In order to avoid half lambda spacing rules, Rule 6.2 is disabled, instead 6.2b, 6.5b, 6.6b, 6.7b, 6.8b are enabled in addition to rules 6.1, 6.3, 6.4. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.





SCMOS Layout Rules - Metal1

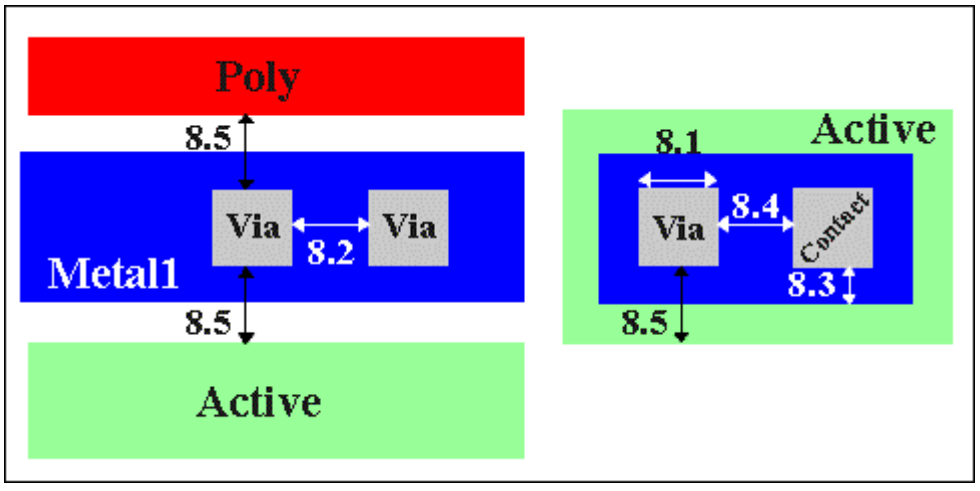
Rule	Description	SUBM	
		Lambda	Microns
7.1	Minimum width	3	0.9
7.2	Minimum spacing	3	0.9
7.3	Minimum overlap of any contact	1	0.3
7.4	Minimum spacing when either metal line is wider than 10 lambda	6	1.8



SCMOS Layout Rules - Via

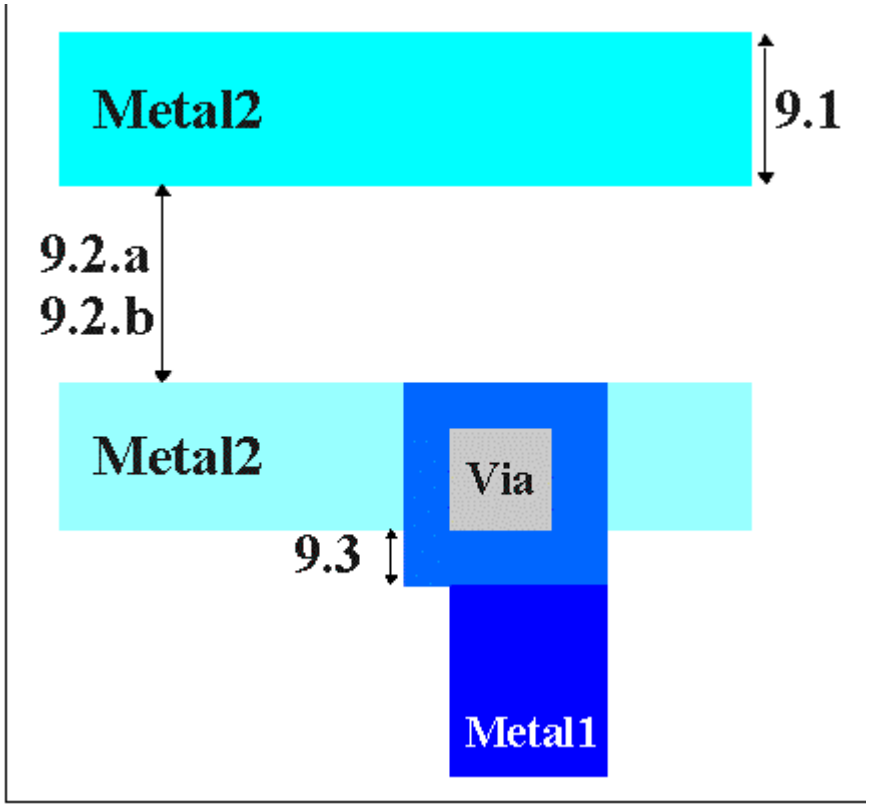
Rule	Description	SUBM	
		3+ Metal Process	
		Lambda	Microns
8.1	Exact size	2 x 2	0.6x0.6
8.2	Minimum via1 spacing	3	0.9
8.3	Minimum overlap by metal1	1	0.3
8.5	Minimum spacing to poly or active edge	2	0.6

Note: Rule 8.4 is not considered for the process we are using since stacked vias are allowed



SCMOS Layout Rules - Metal2

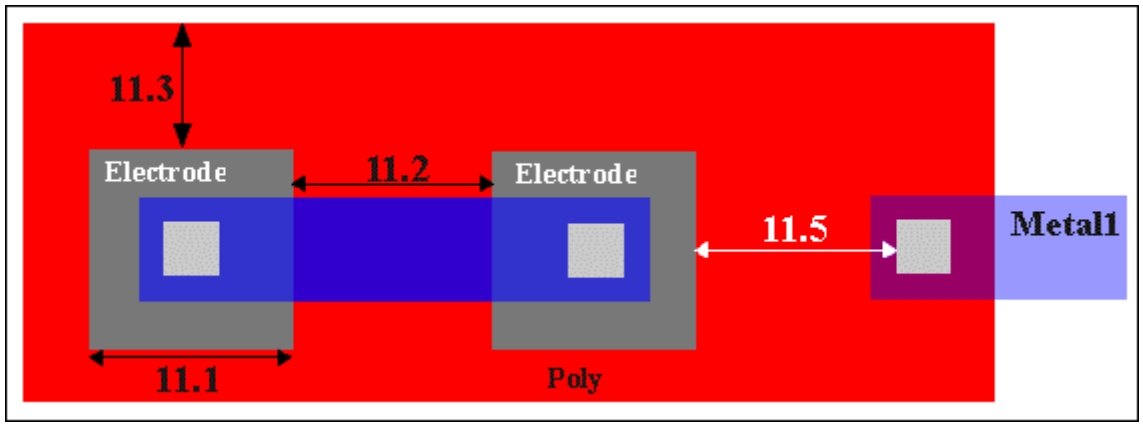
Rule	Description	SUBM	
		3+ Metal Process	
		Lambda	Microns
9.1	Minimum width	3	0.9
9.2	Minimum spacing	3	0.9
9.3	Minimum overlap of via1	1	0.3
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	1.8



SCMOS Layout Rules - Poly2 for Capacitor

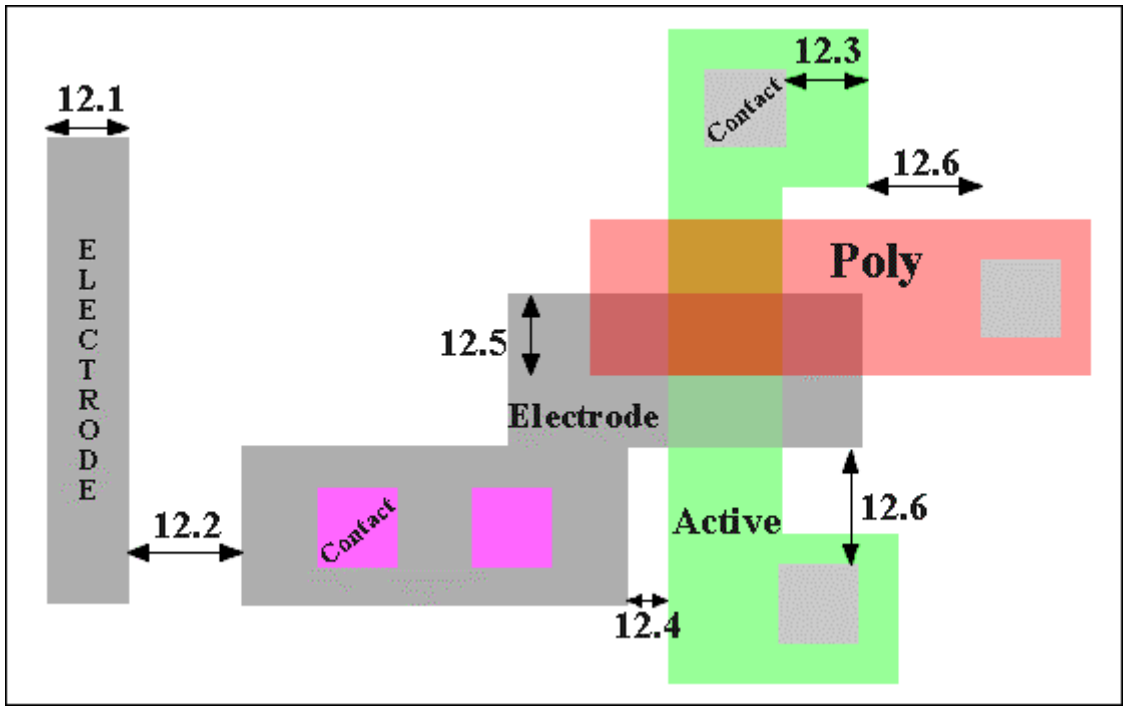
The poly2 layer is a second polysilicon layer (physically above the standard, or first, poly layer). The oxide between the two polys is the capacitor dielectric. The capacitor area is the area of coincident poly and electrode.

Rule	Description	SUBM	
		Lambda	Microns
11.1	Minimum width	7	1.2
11.2	Minimum spacing	3	0.9
11.3	Minimum poly overlap	5	1.5
11.4	Minimum spacing to active or well edge (not illustrated)	2	0.6
11.5	Minimum spacing to poly contact	6	1.8
11.6	Minimum spacing to *unrelated* metal	2	0.6



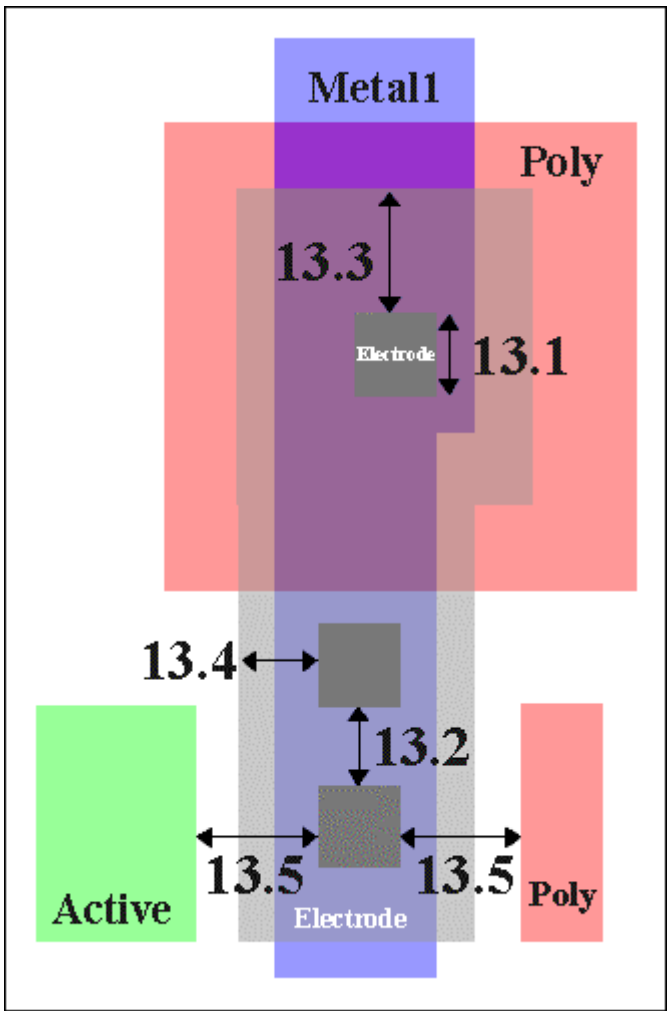
SCMOS Layout Rules - Poly2 for Transistor
Same poly2 layer as for caps

Rule	Description	SUBM	
		Lambda	Microns
12.1	Minimum width	2	0.6
12.2	Minimum spacing	3	0.9
12.3	Minimum electrode gate overlap of active	2	0.6
12.4	Minimum spacing to active	1	0.3
12.5	Minimum spacing or overlap of poly	2	0.6
12.6	Minimum spacing to poly or active contact	3	0.9



SCMOS Layout Rules - Poly2 Contact

Rule	Description	SUBM	
		Lambda	Microns
13.1	Exact contact size	2 x 2	0.6x0.6
13.2	Minimum contact spacing	3	0.9
13.3	Minimum electrode overlap (on capacitor)	3	0.9
13.4	Minimum electrode overlap (not on capacitor)	2	0.6
13.5	Minimum spacing to poly or active	3	0.9

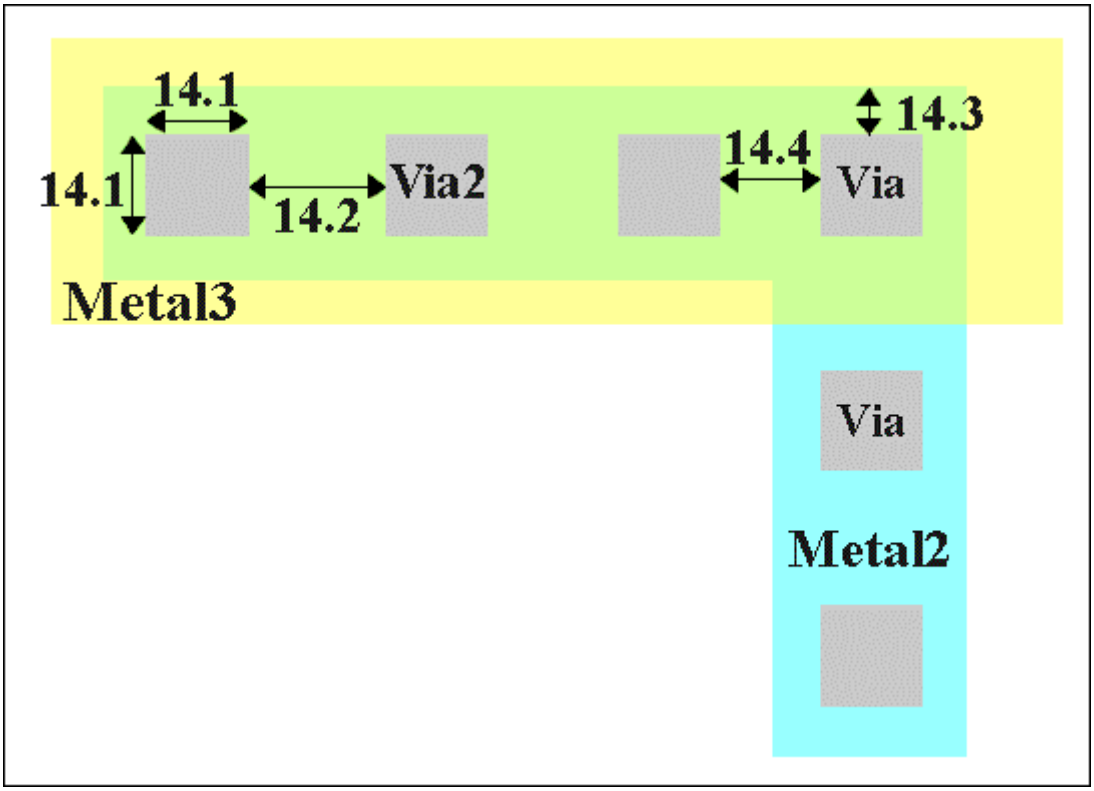


SCMOS Layout Rules - Via2

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

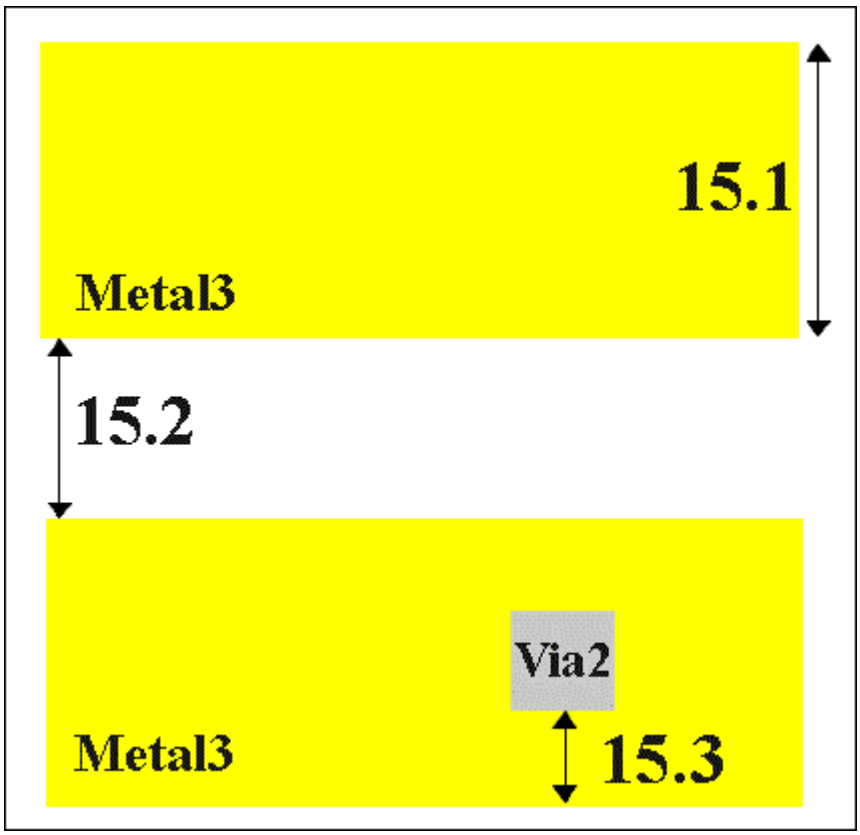
Rule	Description	SUBM	
		3 Metal Process	
		Lambda	Microns
14.1	Exact size	2x2	0.6x0.6
14.2	Minimum spacing	3	0.9
14.3	Minimum overlap by metal2	1	0.3
14.5	Via2 may be placed over contact		

Note: Rule 14.4 is not considered for the process we are using since stacked vias are allowed



SCMOS Layout Rules - Metal3

Rule	Description	SUBM	
		3 Metal Process	
		Lambda	Microns
15.1	Minimum width	5	1.5
15.2	Minimum spacing to metal3	3	0.9
15.3	Minimum overlap of via2	2	0.6
15.4	Minimum spacing when either metal line is wider than 10 lambda	6	1.8



SCMOS Layout Rules - High Res

Rule	Description	SUBM	
		Lambda	Microns
27.1	Minimum HR width	4	1.2
27.2	Minimum HR spacing	4	1.2
27.3	Minimum spacing, HR to contact (no contacts allowed inside HR)	2	0.6
27.4	Minimum spacing, HR to external active	2	0.6
27.5	Minimum spacing, HR to external poly2	2	0.6
27.6	Resistor is poly2 inside HR; poly2 ends stick out for contacts, the entire resistor must be outside well and over field		
27.7	Minimum poly2 width in resistor	5	1.5
27.8	Minimum spacing of poly2 resistors (in a single HR region)	7	2.1
27.9	Minimum HR overlap of poly2	2	0.6

SCMOS Layout Rules - Overglass

Note that rules in this section are in units of microns. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.

Rule	Description	Microns
10.1	Minimum bonding passivation opening	60
10.2	Minimum probe passivation opening	20
10.3	Pad metal overlap of passivation	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to active, poly or poly2	15